In the Claims

1. (Previously Presented) A method of operating an electronic device comprising:

storing data by changing charge on a storage electrode configured such that an energy barrier at an interface between the storage electrode and an adjacent insulator has a barrier energy of less than approximately 1.8 eV, the storage electrode having an electron affinity less than 3.7 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

2. (Original) The method of claim 1, wherein storing data by changing charge on a storage electrode includes storing data by changing charge on the storage electrode adjacent to another insulator having a permittivity higher than a permittivity of silicon dioxide.

3. (Original) The method of claim 1, wherein storing data by changing charge on the storage electrode transconductively provides an amplified signal between ends of a current path above which the storage electrode is disposed.

4. (Original) The method of claim 1, wherein the method further includes reading data by detecting a current flowing through a current path above which the storage electrode is disposed.

5. (Original) The method of claim 4, wherein detecting a current is based on charge on the storage electrode and a transconductance gain of a component element that includes the storage electrode.

6. (Original) The method of claim 1, wherein the method further includes operating with a write/erase time of less than about 1 second.

7. (Original) The method of claim 1, wherein the method further includes operating with a write/erase time of less than about 1 millisecond.

8. (Original) The method of claim 1, wherein the method further includes applying less than 12 volts to a control electrode to erase the charge on the storage electrode.

9. (Original) The method of claim 1, wherein the method further includes operating with a data charge retention time of about 40 seconds.

10. (Original) The method of claim 1, wherein the method further includes operating with a data charge retention time of about 40 seconds at a temperature of about 250°C.

11. (Original) The method of claim 1, wherein operating an electronic device includes operating a system having a processor that sends data that is stored on the storage electrode.

12. (Previously Presented) A method of operating an electronic device comprising:

storing data by changing charge on a floating gate of a floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.8 eV, the floating gate having an electron affinity less than 3.7 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

13. (Original) The method of claim 12, wherein storing data by changing charge on a floating gate includes storing data by changing charge on the floating gate having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

14. (Original) The method of claim 12, wherein the method further including providing a reference potential to a source of the floating gate transistor.

15. (Original) The method of claim 12, wherein storing data includes providing a control voltage to a control gate of the floating gate transistor and providing a write voltage to a drain of the floating gate transistor to change charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

16. (Original) The method of claim 12, wherein the method further includes placing a read voltage to a control gate of the floating gate transistor and detecting a current conducted between a source of the floating gate transistor and a drain of the floating gate transistor.

17. (Original) The method of claim 16, wherein detecting a current includes detecting a data charge signal of about 1000 fC.

18. (Original) The method of claim 16, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

19. (Original) The method of claim 18, wherein detecting a change in current includes sampling or integrating over a time period.

20. (Currently Amended) The method of claim 19, wherein sampling or integrating over a time period ~~over a time period~~ includes sampling or integrating over about 10 nanoseconds.

21. (Original) The method of claim 12, wherein operating an electronic device includes operating a system having a processor that sends data that is stored by changing charge on the floating gate.

22. (Previously Presented) A method of operating a memory comprising:

activating a floating gate transistor, the floating gate transistor including a floating gate having an electron affinity less than 2.7 eV, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.8 eV, the method including:

providing a control voltage to a control gate of the floating gate transistor to store data by changing charge on the floating gate;

detecting a current between a drain of the floating gate transistor and a source of the floating gate transistor at a data line coupled to the drain; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

23. (Original) The method of claim 22, wherein activating a floating gate transistor includes activating the floating gate transistor having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

24. (Original) The method of claim 22, wherein the method further includes providing a write voltage to a drain of the floating gate transistor to change the charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

25. (Original) The method of claim 22, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

26. (Original) The method of claim 25, wherein detecting a change in current includes sampling or integrating over about 10 nanoseconds.

27. (Original) The method of claim 22, wherein the method further includes operating the memory with a write/erase time of less than about 1 millisecond.

28. (Original) The method of claim 22, wherein the method further includes applying less than 12 volts to the control gate of the floating gate transistor to erase the charge on the storage electrode.

29. (Original) The method of claim 22, wherein the method further includes operating the memory with a data charge retention time of about 40 seconds.

30. (Original) The method of claim 22, wherein operating a memory includes sending data for storage in the memory under control of a processor.

31. (Previously Presented) A method of operating a memory comprising:

activating a floating gate transistor, the floating gate transistor including a floating gate having an electron affinity less than 2.5 eV, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.6 eV, the method including:

providing a control voltage to a control gate of the floating gate transistor to store data by changing charge on the floating gate;

detecting a current between a drain of the floating gate transistor and a source of the floating gate at a data line coupled to the drain; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

32. (Original) The method of claim 31, wherein activating a floating gate transistor includes activating the floating gate transistor having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

33. (Original) The method of claim 31, wherein the method further includes providing a write voltage to a drain of the floating gate transistor to change the charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

34. (Original) The method of claim 31, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

35. (Original) The method of claim 34, wherein detecting a change in current includes sampling or integrating over about 10 nanoseconds.

36. (Original) The method of claim 31, wherein operating a memory includes sending data for storage in the memory under control of a processor.

37. (Original) A method of operating a memory comprising:

storing data by changing charge on a floating gate of a floating gate transistor, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.8 eV, the floating gate having an electron affinity smaller than an electron affinity of polysilicon, the electron affinity of polysilicon being approximately 4.2 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

38. (Original) The method of claim 37, wherein storing data by changing charge on a floating gate includes storing data by changing charge on the floating gate having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

39. (Original) The method of claim 37, wherein storing data includes providing a control voltage to a control gate of the floating gate transistor and providing a write voltage to a drain of the floating gate transistor to change charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

40. (Original) The method of claim 37, wherein the method further includes placing a read voltage to a control gate of the floating gate transistor and detecting a current conducted between a source of the floating gate transistor and a drain of the floating gate transistor.

41. (Original) The method of claim 40, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

42. (Original) The method of claim 41, wherein detecting a change in current includes sampling or integrating over about 10 nanoseconds.

43. (Original) The method of claim 37, wherein the method further includes operating the memory with a data charge retention time of about 40 seconds at about 250°C.

44. (Original) The method of claim 37, wherein operating a memory includes sending control signals to the memory from a processor.

45. (Original) A method of operating a memory comprising:

storing data by changing charge on a floating gate of a floating gate transistor, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 0.8 eV, the floating gate having an electron affinity smaller than an electron affinity of polysilicon, the electron affinity of polysilicon being approximately 4.2 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

46. (Original) The method of claim 45, wherein storing data by changing charge on a floating gate includes storing data by changing charge on the floating gate having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

47. (Original) The method of claim 45, wherein storing data includes providing a control voltage to a control gate of the floating gate transistor and providing a write voltage to a drain of the floating gate transistor to change charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

48. (Original) The method of claim 45, wherein the method further includes placing a read voltage to a control gate of the floating gate transistor and detecting a current conducted between a source of the floating gate transistor and a drain of the floating gate transistor.

49. (Original) The method of claim 45, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

50. (Original) The method of claim 49, wherein detecting a change in current includes sampling or integrating over a period of time.

51. (Original) The method of claim 45, wherein operating a memory includes providing addresses from a processor.

52. (Previously Presented) A method of operating an electronic system comprising:

sending an address from a processor to a memory;

sending data to the memory under the control of the processor;

storing data in one or more memory cells of the memory, storing data in each memory cell including changing charge on a floating gate of a floating gate transistor in each memory cell, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and a gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.8 eV, the floating gate having an electron affinity less than 2.7 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

53. (Original) The method of claim 52, wherein storing data by changing charge on a floating gate includes storing data by changing charge on the floating gate having an intergate dielectric disposed on the floating gate, the intergate dielectric having a permittivity higher than a permittivity of silicon dioxide.

54. (Original) The method of claim 52, wherein storing data includes providing a control voltage to a control gate of the floating gate transistor and providing a write voltage to a drain of the floating gate transistor to change charge on the floating gate by hot electron injection or Fowler-Nordheim tunneling.

55. (Original) The method of claim 52, wherein the method further includes placing a read voltage to a control gate of the floating gate transistor and detecting a current conducted between a source of the floating gate transistor and a drain of the floating gate transistor.

56. (Original) The method of claim 52, wherein detecting a current includes detecting a change in current related to an absence or presence of charge stored on the floating gate.

57. (Original) The method of claim 52, wherein changing charge on a floating gate of a floating gate transistor includes changing the charge on the floating gate of the floating gate transistor configured such that the energy barrier at an interface between the floating gate and the gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 2.8 eV.

58. (Previously Presented) A method of operating an electronic system comprising:

sending an address from a processor to a memory;

sending data to the memory under the control of the processor;

storing data in one or more memory cells of the memory, storing data in each memory cell including changing charge on a floating gate of a floating gate transistor in each memory cell, the floating gate transistor configured such that an energy barrier at an interface between the

floating gate and the gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 1.8 eV, the floating gate having an electron affinity smaller than an electron affinity of polysilicon, the electron affinity of polysilicon being approximately 4.2 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

59. (Previously Presented) A method of operating an electronic system comprising:

sending an address from a processor to a memory;

sending data to the memory under the control of the processor;

storing data in one or more memory cells of the memory, storing data in each memory cell including changing charge on a floating gate of a floating gate transistor in each memory cell, the floating gate transistor configured such that an energy barrier at an interface between the floating gate and the gate insulator on which the floating gate is disposed has a barrier energy of less than approximately 0.8 eV, the floating gate having an electron affinity smaller than an electron affinity of polysilicon, the electron affinity of polysilicon being approximately 4.2 eV; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

60. (Previously Presented) The method of claim 1, wherein the storage electrode includes a non-metal storage electrode.

61. (Previously Presented) The method of claim 12, wherein the floating gate includes a non-metal floating gate.

62. (Previously Presented) The method of claim 22, wherein the floating gate includes a non-metal floating gate.

63. (Previously Presented) The method of claim 31, wherein the floating gate includes a non-metal floating gate.

64. (Previously Presented) The method of claim 52, wherein the floating gate includes a non-metal floating gate.